SECTION I. (AMENDMENTS TO THE CLAIMS)

A listing of claims 1-140 of the present application, which are amended herein with markings to show changes made, is provided below:

1-88. (Cancelled).

89. (Currently amended) A layered structure for forming a Ge channel field effect transistors comprising:

a single crystalline substrate,

a first layer of relaxed $Si_{1-x}Ge_x$ formed epitaxially on said substrate where Ge fraction x ~~is the range~~ ranges from about 0.5 to about 0.8,

a second layer of Ge formed epitaxially on said first layer whereby said second layer is under compressive strain and having a thickness less than its critical thickness with respect to said first layer,

a third layer of undoped $Si_{1-x}Ge_x$ formed epitaxially on said second layer, and

a fourth layer of gate dielectric formed on said third layer.

90. (Original) The layered structure of claim 89 further including first and second over-shoot layers, $Si_{1-m}Ge_m$ and $Si_{1-n}Ge_n$, within a strain relief structure of said first layer of relaxed $Si_{1-x}Ge_x$ for the case when x is greater than 0.5.

91. (Original) The layered structure of claim 89 wherein said first over-shoot layer, $Si_{1-m}Ge_m$, within said strain relief structure of said first layer has a Ge fraction m, where m is the range from 0.05 to less than 0.5.

92. (Original) The layered structure of claim 89 wherein said second over-shoot layer, $Si_{1-n}Ge_n$, within the strain relief structure of said first layer has a Ge fraction n, where $n = x + z$ and z is in the range from 0.01 to 0.1, and having a thickness less than its critical thickness with respect to said first layer.

93. (Original) The layered structure of claim 89 wherein the active device region is a buried channel made up of an epitaxial Ge channel of said second layer having a higher compressive strain to provide a deeper quantum well or a higher barrier for better hole confinement with no alloy scattering as compared to a single SiGe layer channel device alone.

94. (Original) The layered structure of claim 89 wherein the Ge content of said third layer of $Si_{1-x}Ge_x$ is in the range from 0.5 to 0.8 with a preferred content of 0.30 and wherein said third layer is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer with a thickness equal to or less than 1 nm.

95. (Original) The layered structure of claim 89 wherein the Ge content x may be graded within said third layer starting with a higher Ge content nearer said second layer and grading down in Ge content towards the upper surface of said third layer to a value of about 0.30.

96. (Original) The layered structure of claim 89 wherein the gate dielectric of said fourth layer is a dielectric material selected from the group consisting of silicon dioxide, silicon

oxynitride, silicon nitride, tantalum oxide, barium strontium titanate, aluminum oxide and combinations thereof.

97. (Original) The layered structure of claim 89 wherein said third layer of $Si_{1-x}Ge_x$ may be substituted with a thin strained commensurate Si layer suitable for high temperature oxidation in formation of a high quality silicon dioxide layer in said fourth layer of gate dielectric.

98. (Original) The layered structure of claim 97 wherein said third layer of Si is under tensile strain and is commensurate having a thickness below its critical thickness with respect to said first layer at its interface with said second layer.

99-123. (Cancelled).

124. (Original) The layered structure of claim 89 further including,

electrical isolation regions created by the selective removal of at least said fourth layer

through said second layer,

a gate electrode formed on said gate dielectric of said fourth layer,

a source electrode formed and located on one side of said gate electrode, and

a drain electrode formed and located on the other side of said gate electrode whereby a field-effect transistor structure is formed.

125-129. (Cancelled).

130-140. (Cancelled).